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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MATTHIAS MUTH

Appeal 2009-002172
Application 10/534,164[1]
Technology Center 2100

Decided: January 8, 2010

Before JAMES D. THOMAS, LEE E. BARRETT, and JOHN A. JEFFERY, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-6. We have jurisdiction pursuant to 35 U.S.C. § 6(b).

We affirm.

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[1] Filed May 5, 2005, titled "Integrated Circuit with LIN-Protocol Transmission," which is a national stage application under 35 U.S.C. § 371 of PCT/IB2003/04838, filed October 30, 2003.

STATEMENT OF THE CASE

The invention

The invention relates to an integrated circuit for a slave node that communicates with a vehicle data bus using a LIN (Local Interconnect Network) bus protocol. The integrated circuit performs clock rate detection and synchronization without an external microcontroller. Spec. 1, ll. 1-27.

Representative claim

Claim 1, the sole independent claim, is reproduced below:

> 1. An integrated circuit having a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset and a monitoring function,
>
> an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN (Local Interconnect Network) protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte,
>
> a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

The references relied upon by the Examiner

Werle	5,778,002	Jul. 7, 1998
Bongiorno	US 6,292,045 B1	Sept. 18, 2001
Feuerstraeter	US 2003/0058894 A1	Mar. 27, 2003 (filed Sep. 20, 2001)
Ishikuri	US 6,674,681 B2	Jan. 6, 2004 (filed Jul. 3, 2002)

Appellant's admitted prior art ("AAPA") at Spec. 1, ll. 9-16.

"Electrical Engineering Glossary Definition for V_{CC}," http://www.maxim-ic.com/glossary.index.cfm/Ac/V/ID/943/Tm/VEE/In/en (11/5/2007).

The rejections

Claims 1 and 6 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Feuerstraeter, AAPA, and Ishikuri.

Claims 2 and 3 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Feuerstraeter, AAPA, and Ishikuri, further in view of Bongiorno.

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Feuerstraeter, AAPA, and Ishikuri, further in view of Werle.

Claim groupings

Appellant does not argue the separate patentability of dependent claims 2-6. Accordingly, the rejections of claims 1-6 stand or fall together with the rejection of claim 1.

FINDINGS OF FACT

Appellant's Admitted Prior Art (AAPA)

The Examiner relies on the following description as AAPA:

> A problem that always exists with the asynchronous transmission of data is that a receiver has to set itself to the clock frequency at which the data is transmitted along the data bus. In what is called the LIN (Local Interconnect Network) protocol for example, which is intended for vehicles, the data is transmitted from a master

> node to slave nodes, the slave nodes being able to synchronize themselves with the rate at which the data is transmitted.
>
> To enable synchronization of this kind to take place to the data clock rate, the slave nodes have to be capable of recognizing certain symbols that differ from those employed by a standard SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface. This latter type of interface is one that is used as standard for serial data transmission.

Spec. 1, ll. 7-17.

However, the Specification also describes that the invention "provides the basic functions of a system base chip of the kind that is normally provided for transceivers for vehicle data bus systems. These basic functions comprise at least a system voltage supply, a system reset and a monitoring function such as, for example, a watchdog." Spec. 2, ll. 11-14. Therefore, we find that the functions of the base chip are admitted by Appellant to be well known.

Feuerstraeter

Feuerstraeter describes a method and system for automatically configuring devices for communicating when LAN-configured devices attempt to communicate with WAN-configured devices and vice versa.

Feuerstraeter describe a serializer for receiving bits in parallel and sending them out serially and a deserializer for receiving bits serially and retransmitting them in parallel. ¶¶ [0029]-[0030]. The combination of the serializer and deserializer is called a SERDES. ¶ [0042].

The deserializer 405 shown in Figure 4 has a data rate detection unit 420 for determining the rate of data transfer, i.e., a baud rate. ¶ [0044]. The input data rate is used to automatically configure the serializer to correspond to the detected data rate. ¶ [0047].

The deserializer 505 shown in Figure 5 has a serial-to-parallel converter at the lower left hand side of the box.

The serializer 504 and deserializer 505 shown in Figure 5 are depicted within dashed line blocks having pins, which we find are representative of integrated circuit packages.

PRINCIPLES OF LAW

"[T]he test [for obviousness] is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). A rejection under 35 U.S.C. § 103(a) is based on the following factual determinations: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1360 (Fed. Cir. 2006) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). "[H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

CONTENTIONS

The Examiner finds that AAPA teaches that to enable synchronization between two communicating devices using a LIN protocol, the receiving device would need to be capable of recognizing certain symbols that differ from those utilized by a standard interface. Final Rej. 2. The Examiner finds that AAPA does not teach a system base chip "that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset and a monitoring function" or an "interface circuit" or a "monitoring function" or a "serial/parallel converter," as claimed. *Id.* The Examiner finds that Feuerstraeter teaches a base chip having a transmitting and/or receiving system (which the Examiner considers a monitoring function), and interface circuit that performs bit-rate detection, and a serial/parallel converter. *Id.* at 3. The Examiner finds that Ishikuri teaches an integrated circuit having a system voltage supply and a system reset. *Id.* The Examiner concludes that it would have been obvious to combine Feuerstraeter's teachings of detecting bit-rates with AAPA "for the purpose of automatically detecting a data transfer rate such that one or more devices may communicate with each other when otherwise the devices would not." *Id.* The Examiner further concludes that it would have been obvious to combine Ishikuri's teaching of transmitting and receiving data with AAPA "for the purpose of preventing erroneous operations due to runaway of a system (see Ishikuri, Column 5, lines 6-8)." *Id.* at 4. In the Answer, the Examiner further reasons that it would have been obvious to combine Feuerstraeter with AAPA "for the purpose of being able to more efficiently communicate with a device of a

different protocol by automatically detecting and adjusting for the various differences in the two protocols (e.g., by synchronizing the incoming data by detecting the incoming bit rate, converting between serial and parallel protocols, etc.)." Ans. 5.

Appellant argues: (1) there is no reason to combine the elements in the manner suggested by the Examiner because the devices of the AAPA can communicate and therefore, the Examiner's reasoning that Feuerstraeter would be combined so that the devices "may communicate with each other when otherwise the devices would not" (Final Rej. 3) is erroneous; (2) the Examiner has relied upon hindsight reconstruction because the Examiner has applied a shifting rationale to combining the reference implying that the Examiner has improperly used Appellant's Specification; (3) the asserted combination of references would defeat the purpose of the primary reference because the WAN and LAN protocols of Feuerstraeter would not be capable of receiving and transmitting information using the LIN protocol; and (4) the references fail to teach every limitation of the claimed invention, in particular, the power on clear (POC) circuit of Ishikuri is not a system voltage supply as found by the Examiner. Br. 4-8; Reply Br. 5.

The Examiner concludes in the Answer that "[t]he teachings of Feuerstraeter as described above would eliminate the need for a dedicated external microcomputer to be used to convert (i.e., adapt) between protocols. This would result in less cost to implement the system." Ans. 8.

Appellant argues that the Examiner's new motivation is taken directly from Appellant's disclosure, which is hindsight, and the Examiner has now again shifted the rationale, further indicating hindsight. Reply Br. 3-4.

The Examiner further reasons in the Answer that the AAPA teaches that the LIN protocol was known and "since the components disclosed in Feuerstraeter are not limited to the protocols in Feuerstraeter, implementing the LIN protocol as taught by AAPA with Feuerstraeter would have yielded an expected and predictable result." Ans. 9.

ISSUE

Has Appellant shown that the combination of references would not have suggested the claimed invention?

CLAIM INTERPRETATION

Before we address the patentability rejection, we interpret claim 1. Claim 1 recites:

> An integrated circuit having a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, . . . an interface circuit that . . . runs at least parts of a data bus protocol, . . . , that performs detection of the bit-rate of received data, . . . a serial/parallel converter . . . .

We interpret the word "having" as a transitional word equivalent to "comprising"; the claim could be written with a colon after "having." Thus the integrated circuit comprises: (1) a base chip; (2) an interface circuit; and (3) a serial/parallel converter. This is consistent with the Specification which states that the integrated circuit of the invention has three functional blocks (Spec. 2, ll. 10-11).

Claim 1 does not define the physical structure of the "integrated circuit." Claim 1 does not require that the three elements are on the same

chip; in fact, the recitation of a base chip indicates that the base chip is a separate chip. Although Figure 1 shows the integrated circuit as a block diagram containing all the elements, claim 1 does not require that the integrated circuit is contained in a package. An "integrated circuit" can be made of separate integrated circuit elements, a known base chip and a separate interface circuit and a separate serial/parallel converter circuit. Thus, the term "integrated circuit" in claim 1 does not positively recite that all elements are the same chip or in the same package.

Claim 1 recites an "an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol." It is not clear how the term "self-contained" limits the structure of claim 1. The statement that the "interface circuit . . . runs at least parts of a data bus protocol" does not state how much of the protocol is run by the interface circuit. We understand that the prior art uses an external microcontroller for the interface (Spec. 1, ll. 20-22), but apparently a microcontroller can still be used as long as it is not completely responsible for running the data bus protocol.

ANALYSIS

The Examiner finds that the AAPA does not teach a system base chip "that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset and a monitoring function," Final Rej. 2, and applies Ishikuri for teaching an integrated circuit having a system voltage supply and a system reset, *id.* at 3. However, the Specification describes that the invention "provides the basic functions of a system base chip of the kind that is normally provided for

transceivers for vehicle data bus systems. These basic functions comprise at least a system voltage supply, a system reset and a monitoring function such as, for example, a watchdog." Spec. 2, ll. 11-14. Thus, a base chip as claimed is in the AAPA. Although the Examiner errs in finding that the AAPA does not describe a system base chip, and errs in finding that Ishikuri teaches a system voltage supply for the reasons stated by Appellant at Br. 7-8, the AAPA nevertheless teaches the recited functions. Thus, we find that the AAPA teaches "a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset and a monitoring function," as claimed, and that these are required functions. Ishikuri is not needed for these limitations.

The Examiner finds that Feuerstraeter teaches a base chip having a transmitting and/or receiving system (which the Examiner considers a monitoring function) using a bus protocol, and interface circuit which performs bit-rate detection, and a serial/parallel converter. Final Rej. 3. Appellant does not dispute that Feuerstraeter teaches an integrated circuit having an interface circuit that runs a bus protocol and detects the bit-rate of the received data and performs serial/parallel conversion using the detected bit-rate. Figure 5 of Feuerstraeter shows the serializer 504 and deserializer 505 enclosed within dashed lines and pin inputs/outputs and thus teaches the system is at least in a package, if not on a chip. The Examiner errs in finding that the transceiver performs a monitoring function, but this is harmless error since the system base chip of the AAPA performs a monitoring function (*see* Spec. 2, ll. 13-14).

At this point in the analysis, we have the AAPA which teaches a system base chip for a LIN protocol having a system voltage supply, a system reset, and a monitoring function, and Feuerstraeter which teaches a deserializer having an interface circuit that runs a serial bus protocol and detects the bit-rate of received data and a serial/parallel converter. The specific issues are whether one of ordinary skill in the art would have been motivated to: (1) utilize the interface and serial/parallel teachings of Feuerstraeter with a LIN protocol; and (2) combine the functionality of Feuerstraeter with the system base chip functions in the AAPA in an integrated circuit.

The Examiner finds that the AAPA teaches that to enable synchronization between two communicating devices using a LIN protocol, the receiving device would need to be capable of recognizing certain symbols that differ from those utilized by a standard interface. Final Rej. 2. The Examiner concludes that it would have been obvious to combine Feuerstraeter's teachings of detecting bit-rates with AAPA "for the purpose of automatically detecting a data transfer rate such that one or more devices may communicate with each other when otherwise the devices would not." Final Rej. 3; Ans. 8. Appellant argues that the Examiner's reasoning is erroneous because the AAPA devices can communicate, that the Examiner has applied a shifting rationale to combining the reference implying that the Examiner has improperly used Appellant's Specification, and that the asserted combination of references would defeat the purpose of the AAPA because the WAN and LAN protocols of Feuerstraeter would not be capable of receiving and transmitting information using the LIN protocol.

The AAPA describes serial data transmission and the problem of synchronization to different data rates in the LIN bus protocol. Feuerstraeter describes one solution to the problem of synchronization of different data rates on a serial bus. One of ordinary skill in the art looking for a solution to the problem of synchronization to different data rates over a serial data bus in the prior art would have looked to Feuerstraeter for a solution. Similarly, if one required a parallel output from a serial bus, it would have been obvious to use a serial/parallel converter as taught by Feuerstraeter. Thus, the motivation for the providing the functionality of Feuerstraeter in a LIN protocol is not based on impermissible hindsight. "One of the ways in which a patent's subject matter can be proved obvious is by noting there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims." *KSR*, 550 U.S. at 419-20. The Examiner's statement that devices would not otherwise communicate is not well stated, but is apparently is only meant to repeat the statement in Feuerstraeter ¶ [0011], lines 3-4, and to say that detecting a data rate is necessary for communication, not that the prior art was incapable of communication. It is not clear why the Examiner relies on the statement in the AAPA that devices using a LIN protocol need to be able to recognize certain symbols that differ from a standard interface since this fact is apparently never used in the rejection. Although Feuerstraeter does not use the LIN bus protocol, one skilled in the art had the necessary skill to adapt the system of Feuerstraeter to any serial protocol including a LIN protocol.

The next question is whether it would have been obvious to combine the functionality of Feuerstraeter with the system base chip functions in the

AAPA. Feuerstraeter shows the functions of an interface that runs a serial data bus protocol with baud-rate determination and a serial/parallel converter. These functions are "self-contained" in an integrated circuit package as indicated in Figure 5. The AAPA also describes normal support functions of a base chip, which is also an integrated circuit. Although not discussed by the Examiner, it appears from the Specification and claim 1 that the invention is directed to combining the functions of the interface and serial/parallel converter with the functions of the AAPA base chip in the same broadly defined "integrated circuit" so that one "integrated circuit" integrates several necessary LIN protocol functions. That is, it appears that the functions of the baud-rate determination and serial/parallel conversion had to be known in the prior art, but were performed by an external microcontroller. We find that those of ordinary skill in the electronics art were generally motivated to combine related functions in an integrated circuit for the purpose of simplifying the ultimate system design, i.e., so that circuit designers could specify one integrated circuit rather than having to combine several circuits. We conclude that it would have been obvious to combine the interface and serial/parallel functions of Feuerstraeter with the functions of the AAPA base chip as an "integrated circuit" to simplify the design and because the combination does not produce any different results.

The Examiner concludes in the Answer that "[t]he teachings of Feuerstraeter as described above would eliminate the need for a dedicated external microcomputer to be used to convert (i.e., adapt) between protocols. This would result in less cost to implement the system." Ans. 8. We agree with Appellant that this reasoning sounds like an impermissible use of

Appellant's Specification. However, there is adequate reason to combine Feuerstraeter with the AAPA to put all the communication and base chip functions in a single integrated circuit to simplify the design. As to the Specification's description of eliminating the need for an "external microcontroller," Spec. 1, ll. 25-27, claim 1 does not define the structure of the integrated circuit to be a single chip or package so as to define a boundary between what is "internal" and what is "external." Nevertheless, even if claimed, Feuerstraeter shows the deserializer and serializer functions in self-contained packages and one of ordinary skill in the art would have been motivated to combine the circuits of Feuerstraeter with the support circuits of the base chip of the AAPA because it was well known in the semiconductor art to integrate functions in a package or chip.

CONCLUSION

Appellant has not shown that the combination of references would not have taught or suggested the invention of claim 1. The rejections of claims 1-6 are affirmed.

Requests for extensions of time are governed by 37 C.F.R. § 1.136(b). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

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